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Deep RIE Process for Silicon Carbide Power Electronics and MEMS

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ABSTRACT

Reactive ion etching (RIE) of silicon carbide (SiC) to depths ranging from 10 μm to more than 100 μm is required for the fabrication of SiC power electronics and SiC MEMS. A deep RIE process using an inductively coupled plasma (ICP) etch system has been developed which provides anisotropic etch profiles and smooth etched surfaces, a high rate (3000 Å/min), and a high selectivity (80:1) to the etch mask. An etch depth of 100 μm is demonstrated.

INTRODUCTION

Deep RIE processes for SiC are needed to realize the intrinsic advantages of SiC for power electronics and harsh environment MEMS. Etch depths from 10 μm to more than 100 μm are required for trench isolation of SiC power devices, through-wafer vias for advanced packaging schemes, and bulk micromachined SiC structures. The ideal deep RIE process would provide a high rate (at least several thousand Å/min), a highly anisotropic etch profile (e.g. vertical sidewalls with minimal bowing), and smooth etched surfaces. In addition, a high selectivity with respect to an easily deposited and patterned etch mask is required. Deep RIE of SiC has previously been demonstrated using conventional capacitive-type RIE systems [1]. Previously, inductively coupled plasma (ICP) etching has been shown to provide high rates for SiC [2-4]. The effectiveness of ICP for deep etching of SiC is demonstrated here.

Key advantages of ICP relative to conventional RIE include: (1) a considerably higher plasma density, which provides a greater flux of energetic ions and reactive species (e.g. atomic fluorine) to the sample; (2) capability for operation at lower pressures, which helps minimize bowing of the etch sidewalls and can also help to eliminate residues caused by the redeposition of nonvolatile etch products (e.g. sputtered mask materials) onto the etched surfaces; (3) capability for independent control of the plasma density and the energy with which ions bombard the sample, through the use of separate RF generators for the coil and substrate bias electrode.

EXPERIMENT A: ETCH RATE AND SELECTIVITY MEASUREMENTS

For this study deep ICP etching was performed on the silicon face of n-type 6H-SiC using an STS Multiplex ICP [5]. The 10-mm square SiC samples were attached to 100-mm diameter silicon carrier wafers using a drop of photoresist. Typically, the silicon carrier wafer etches at a fairly rapid rate (about 2 μm/min) because Si readily reacts to form a volatile product with atomic fluorine. The sacrificial carrier wafer helps to minimize roughness caused by the sputtering of nonvolatile materials onto the etched SiC surface, which leads to micromasking. The loading effect caused by the silicon carrier wafer varies with different process parameters. For the baseline process (described below), the same etch rate was obtained whether the SiC

sample was mounted on a bare silicon wafer or a silicon wafer coated with nonreactive indium-tin-oxide (ITO). Nickel was used for thinner (≤2500 Å) and ITO for thicker etch masks (up to 3.5 μm). For thicknesses greater than about 2500 Å, Ni was too highly stressed, while the grain size of the ITO made it unsuitable for thinner masks. Liftoff was found to be a convenient means to pattern these evaporated films.

A series of experiments was performed to determine the effects on SiC etch rate and selectivity that would be produced when the pressure, platen power (power to the substrate bias electrode) and oxygen flow were varied from the baseline process parameters. The baseline parameters, which were found in a preliminary investigation to provide a clean deep etch, are shown in table 1. A Ni etch mask was used for these measurements.

Table 1. Baseline process parameters:

Pressure	**SF_6 flow**	**O_2 flow**	**Coil power**	**Platen power**
5 mTorr	55 sccm	0	800 W	75 W

Figure 1 shows the SiC etch rate as a function of pressure. Etch rate was found to decrease with increasing pressure. For these measurements the flow rate was maximized subject to the constraints imposed by the pumping system and flow controller. The SF_6 flow was 27 sccm at 3 mTorr, 55 sccm at 5 mTorr, and 110 sccm for 10 mTorr and higher.

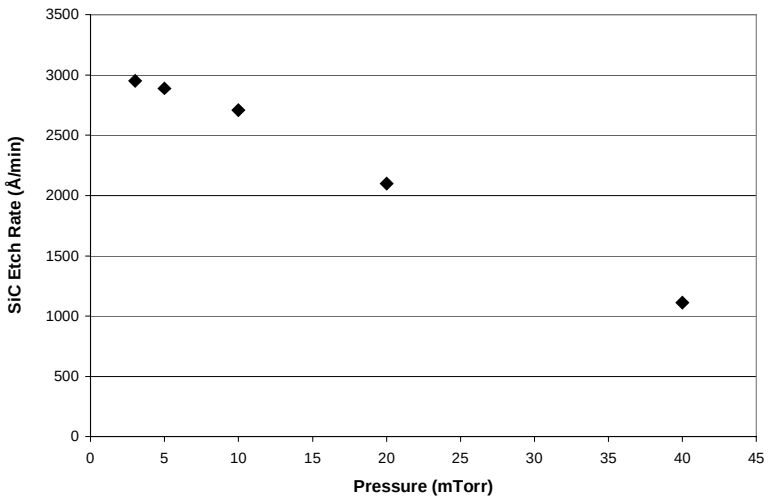

Figure 1. *SiC etch rate as a function of pressure (27-110 sccm SF_6, 800 W coil, 75 W platen).*

Figure 2 shows the SiC etch rate and the selectivity to the Ni mask (ratio of the SiC and Ni etch rates) as functions of the platen power. The application of RF power to the platen causes ions from the plasma to be accelerated towards the substrate. Since the etch mask forms no volatile products with fluorine, its etch rate is strongly influenced by the platen power. For a platen power of 75 W or less, the selectivity is greater than 80:1.

Figure 3 shows the effect of oxygen on the etch rates of SiC and Si. Here, the total flow rate was held fixed at 55 to 60 sccm, while the proportions of SF_6 and O_2 were varied. In general, the SiC etch rate decreased with increasing O_2 fraction. The slight increase in etch rate observed at 64% O_2 coincided with a rapidly decreasing Si etch rate; slower etching of the silicon carrier would make more atomic fluorine available for SiC etch.

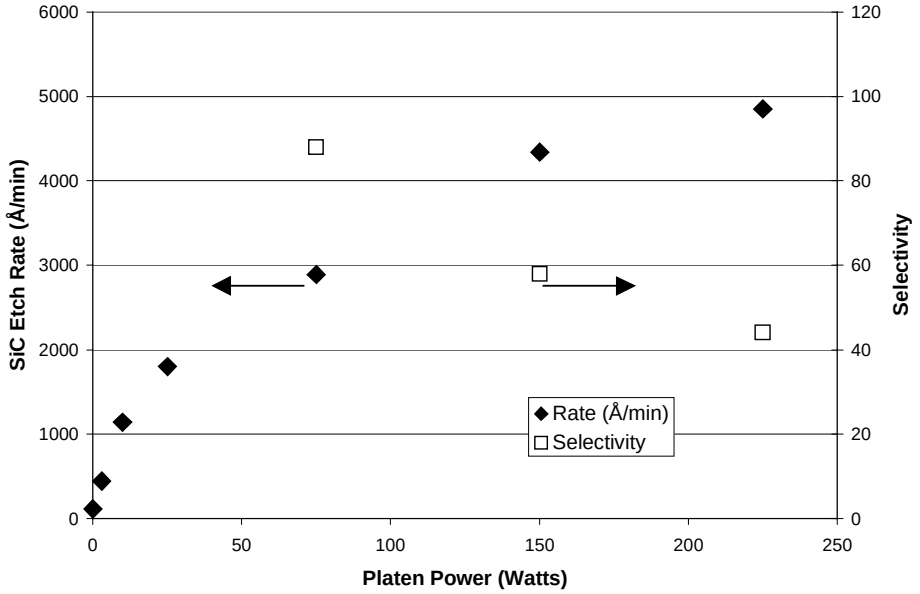

Figure 2. *SiC etch rate and selectivity to Ni mask as functions of platen power (55 sccm SF_6, 5 mTorr pressure, 800 W coil power).*

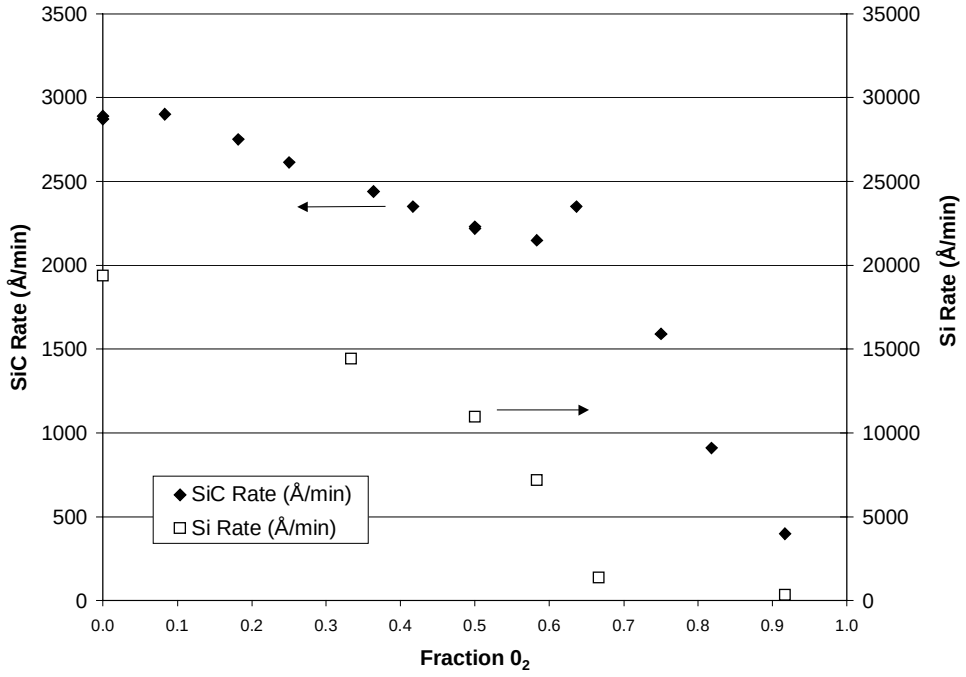

Figure 3. *SiC and Si etch rates as functions of the ratio of the O_2 flow to the total of the SF_6 and O_2 flows (55-60 sccm total flow, 5 mTorr pressure, 800 W coil and 75 W platen power).*

EXPERIMENT B: DEEP ETCHING

An investigation of the various etch parameters for etches deeper than 10 μm found that the baseline process parameters provided a deep etch that was satisfactory for many applications. Relative to the baseline parameters, higher platen powers produced a lower selectivity to the mask, higher pressures and the addition of oxygen promoted residue formation, while lower pressures caused increased trenching. Figure 4 shows typical results for an off-baseline etch using 20 sccm SF_6 and 35 sccm O_2, with all other parameters identical to the baseline. Figure 4 is an SEM image of a 1-mm diameter well which was etched to a depth of 40 μm. The application for this type of etch would be the fabrication of a diaphragm for a high temperature SiC pressure sensor.

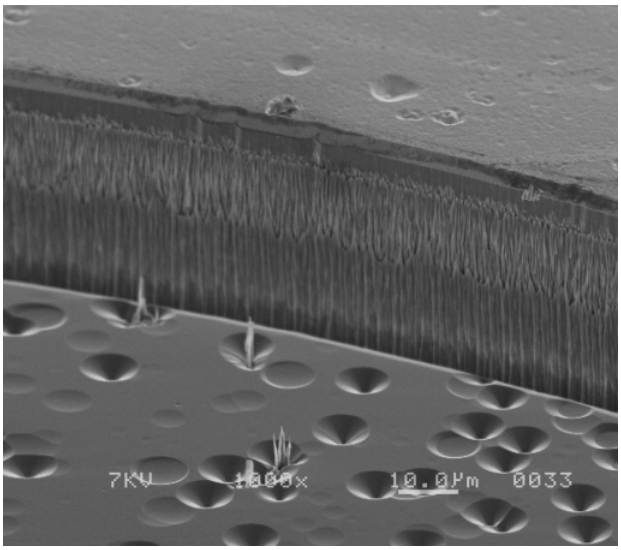

Figure 4. *SEM image of a 1-mm diameter pit etched 40 μm using 20 sccm SF_6 and 35 sccm O_2, 5 mTorr pressure, 800 W coil and 75 W platen power.*

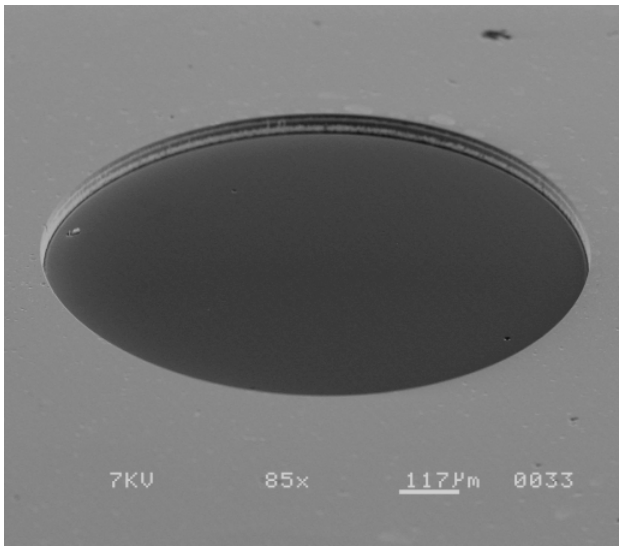

Figure 5. *SEM image of a 1-mm diameter pit etched 46 μm using 55 sccm SF_6, 5 mTorr pressure, 800 W coil and 75 W platen power.*

The etch mask, which was not stripped prior to the SEM, was 3.5-μm thick ITO, and the duration of the etch was 150 min. The spike-like etch residue visible in Figure 4 was found to be almost entirely eliminated when the baseline parameters (55 sccm SF_6, no O_2) were used. The dimples in the etched surface, however, were a characteristic common to all the etch recipes which were tried. This texturing of the etched surface was found to be primarily determined by the condition of the SiC surface at the beginning of the etch. Organic residues and scratches, for example, were found to produce a high concentration of dimples. A number of cleaning procedures (solvents, hot sulfuric, oxidation followed by HF etch) were tried but none was found satisfactory. Several plasma cleaning processes, however, were found to be effective. Figure 5 shows an SEM of a 1-mm diameter pit etched to a depth of 46 μm using the baseline etch process (55 sccm SF_6, no O_2). Again the mask was 3.5 μm ITO, and the duration of the etch was 150 min. Prior to initiation of the deep etch process, the sample was sputter etched in the ICP for 10 min using 50 sccm Ar, 2.5 mTorr pressure, 800 W coil and 75 W platen power.

As can be seen in Figure 5, the ICP sputter etch pretreatment almost entirely eliminated the dimples from the etched surface. However, an entirely satisfactory cleaning procedure has not yet been developed. A disadvantage of the ICP sputter clean is the high rate at which it erodes the ITO mask. The 10 min sputter etch in the ICP was found to remove 1 μm of ITO, but only 500 Å of SiC. A higher pressure may provide a more favorable etch ratio. Preliminary results have shown that a sputter clean using conventional RIE can be effective at eliminating surface texture, with significantly less mask erosion.

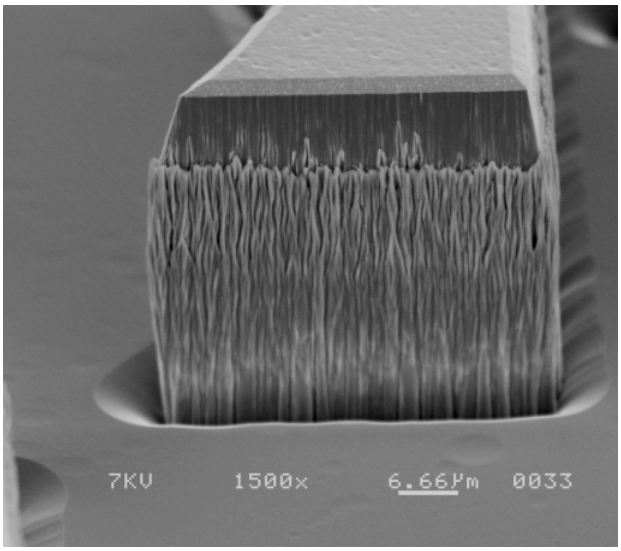

Figure 6. *SEM image of a smaller feature etched in the sample shown in figure 5.*

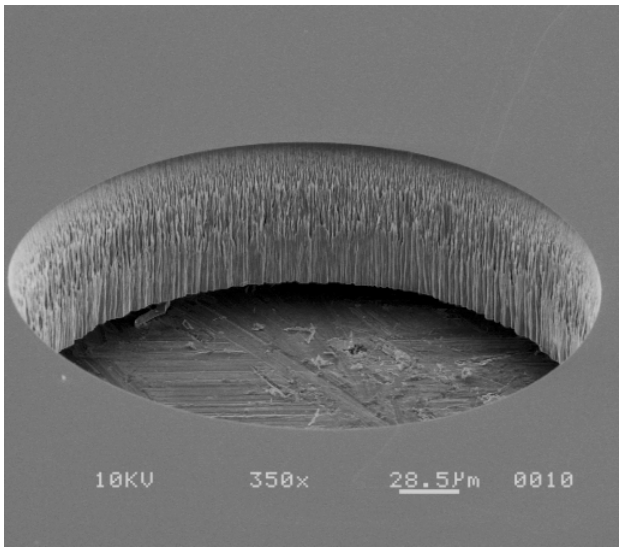

Figure 7. *SEM image of a via etched through a 100 μm thick SiC wafer.*

The baseline deep RIE process, which was used to etch the well shown in figure 5, also provides a satisfactory etch of structures with higher aspect ratios. Figure 6 shows a smaller feature, an alignment mark, from the same sample as is shown in figure 5. The residual ITO mask was not stripped. Enhanced etching (trenching) at the bottom of the sidewalls is caused by the deflection of ions that strike the sidewalls at grazing angles of incidence. The slope of the upper part of the sidewalls was a result of the excessive mask erosion during the sputter etch pretreatment.

The baseline process is well suited for the etching of vias. Figure 7 shows a via etched through a 100-μm thick SiC wafer. The etch mask was 3.5-μm thick ITO which was readily electron-beam evaporated and patterned using by liftoff. The masked side of the wafer is shown here; the residual ITO was stripped prior to electron microscopy. Previously, the deepest SiC plasma etch reported was 80 μm, using conventional RIE [1]. In this case, a thick nickel mask, fabricated using selective electro-deposition, was used.

A highly uniform etch is obtained using the baseline deep RIE process. Figure 8 shows the surface profile of a typical well in the sample shown in figure 5. The etch mask was not yet stripped from this sample. The depth of the well is uniform within ± 2000 Å or ± 0.2% (excluding the trench at the base of the wall, which is inaccessible to the stylus of the profilometer).

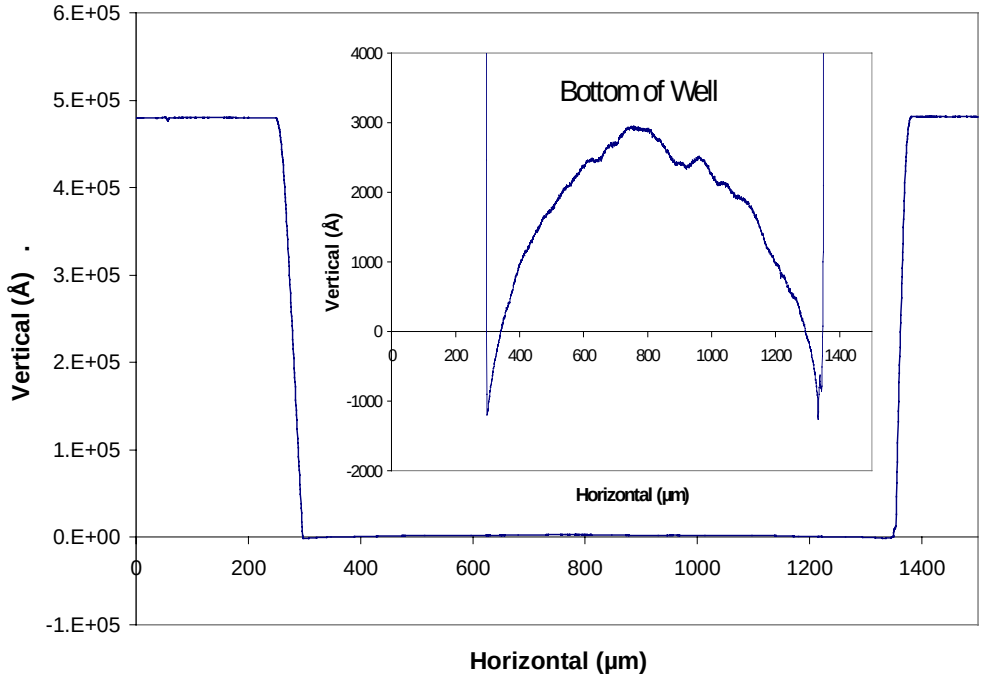

Figure 8. *Surface profile of the bottom of a well etched in the sample shown in figures 5 and 6. The inset shows the bottom of the well using an expanded vertical scale.*

CONCLUDING REMARKS

An ICP etch process for SiC has been developed which meets many of the deep etching requirements for SiC power devices and MEMS. This process provides a high rate (3000 Å/min), vertical sidewalls, smooth etched surfaces, and high selectivity to the etch mask (80:1). Further work is needed to optimize the surface cleaning procedure which precedes the deep etch process. In addition, work is planned to develop a process which produces smoother sidewalls, which are important in some applications, such as mesas for vertical structure high-voltage devices.

ACKNOWLEDGEMENTS

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